

WHAT IS CLAIMED IS:

1. A method comprising the steps of:  
receiving a command at a device through a sequencer that controls  
5 interactions on a small computer system interface bus;  
programming the sequencer to interrupt a co-processor before executing the  
command; and  
executing a set of instructions on the co-processor based on a stored error  
mode page so that a false error condition is generated.  
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2. The method of claim 1 wherein executing a set of instruction comprises  
reprogramming the sequencer so that it is prevented from entering a reselection  
phase to re-establish a connection across the small computer system interface bus.
- 15 3. The method of claim 2 wherein preventing the sequencer from entering a  
reselection phase comprises preventing the sequencer from entering a reselection  
phase to re-establish a connection to transfer data.
4. The method of claim 2 wherein preventing the sequencer from entering a  
20 reselection phase comprises preventing the sequencer from entering a reselection  
phase to re-establish a connection to transfer a status after allowing the sequencer to  
transfer data.
5. The method of claim 1 wherein executing a set of instructions comprises:  
25 setting a reduced data length for a data transfer; and  
setting instructions for the sequencer to enter an indefinite loop after  
completing a data transfer.

6. The method of claim 1 wherein executing a set of instructions comprises replacing the command with an illegal command.
7. The method of claim 1 wherein executing a set of instructions comprises:  
5 determining that the command is a write command;  
instructing the sequencer to execute the write command;  
setting a timer to allow the sequencer to transfer at least one block of data;  
and  
posting a false error when the timer expires.
- 10 8. The method of claim 1 wherein executing a set of instructions comprises reprogramming the sequencer to interrupt the co-processor after a transfer buffer has been filled but before the sequencer begins to transfer data.
- 15 9. The method of claim 8 wherein executing a set of instructions further comprises modifying at least some of the data in the transfer buffer so that the data contains at least one error.
10. A device comprising:  
20 a sequencer adapted to be connected to a small computer system parallel interface bus;  
a co-processor, coupled to the sequencer and capable of being interrupted by the sequencer and of providing instructions to the sequencer; and  
an instruction storage component, communicatively connected to the co-processor and containing processor-executable instructions that are  
25 designed to initiate an error condition after the sequencer sends an interrupt to the co-processor.

11. The device of claim 10 wherein the processor-executable instructions comprise instructions for preventing the sequencer from entering a reselection phase for a period of time so that the sequencer does not establish a connection across the small computer system parallel interface bus.

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12. The device of claim 11 wherein preventing the sequencer from entering a reselection phase comprises preventing the sequencer from entering a reselection phase to establish a connection to transfer data.

10 13. The device of claim 11 wherein preventing the sequencer from entering a reselection phase comprises preventing the sequencer from entering a reselection phase to establish a connection to transfer a status.

14. The device of claim 10 wherein the processor-executable instructions  
15 comprise instructions for:  
    determining a desired data length for data associated with a command;  
    identifying a reduced data length that is less than the desired data length;  
        and  
    instructing the sequencer to execute the command using the reduced data  
20 length.

15. The device of claim 14 wherein the processor-executable instructions further comprise instructions for instructing the sequencer to enter an indefinite loop after executing the command.

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16. The device of claim 10 wherein the processor-executable instructions further comprise instructions for replacing a command with an illegal command.

17. The device of claim 10 wherein the processor-executable instructions further comprise instructions for allowing the sequencer to transfer a portion of a block of data during a write command and generating a false error after the transfer.

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18. The device of claim 10 wherein the processor-executable instruction further comprise instructions for changing data read from a medium before the sequencer transmits the data across the small computer system interface parallel interface bus.

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19. A method comprising:  
receiving a command to generate a false data miscompare error;  
reading data from a storage medium into a memory;  
changing at least some of the data in the memory to form corrupted data;  
15 passing the corrupted data as the data read from the storage medium.

20. A method comprising:  
receiving an indication that a false timeout error should be generated  
during execution of a command;  
20 receiving the command;  
processing a portion of the command; and  
stopping the processing of the command before completing the command  
without indicating that processing of the command has stopped.

25 21. The method of claim 20 wherein receiving a command comprises receiving a read command and wherein processing a portion of the command comprises transferring data.

22. A method comprising:

receiving a command at a storage device to generate a false error, the  
command comprising at least one sense parameter;  
generating a false error message from the storage device that indicates that  
an error has occurred when it has not occurred, the false error  
5 message describing the error in part by including the at least one  
sense parameter.